CLAIMS

[1] A PLL frequency synthesizer comprising:

a voltage control oscillator of changing an oscillation frequency, depending on a potential of an oscillation frequency control signal;

a frequency divider of dividing the oscillation frequency from the voltage control oscillator with a predetermined frequency division ratio;

a phase comparator of receiving an output signal from the frequency divider and an external reference signal, detecting a difference in phase between the output signal and the reference signal, and outputting a phase difference signal;

a charge pump circuit of causing a constant current to flow in or out, depending on the phase difference signal from the phase comparator;

a loop filter of filtering out a high frequency component of an output of the charge pump circuit, converting the current flowing into or out of the charge pump circuit into a voltage, and outputting the voltage as the oscillation frequency control signal; and

a linearization circuit of controlling a conversion gain of the phase comparator and the charge pump circuit so as to compensate for nonlinearity of a loop gain of the PLL frequency synthesizer with respect to the oscillation frequency control signal.

[2] The PLL frequency synthesizer of claim 1, wherein the linearization circuit receives the oscillation frequency control signal from the loop filter, and continuously controls the conversion gain of the phase comparator and the charge pump circuit, depending on the potential of the oscillation frequency control signal.

[3] The PLL frequency synthesizer of claim 2, wherein the linearization circuit has a transistor, a current flowing through the transistor varying depending on the potential of the oscillation frequency control signal from the loop filter, and

the linearization circuit continuously controls the conversion gain of the phase

comparator and the charge pump circuit, depending on a value of the current flowing through the transistor.

[4] The PLL frequency synthesizer of claim 3, wherein the transistor of the linearization circuit is composed of a plurality of transistors, and

the conversion gain of the phase comparator and the charge pump circuit is continuously controlled, depending on a sum of currents flowing through the plurality of transistors.

[5] The PLL frequency synthesizer of claim 4, wherein the plurality of transistors of the linearization circuit have different threshold voltages from each other.

[6] The PLL frequency synthesizer of claim 3, wherein the linearization circuit has a bias voltage generating circuit of generating a bias voltage,

the bias voltage of the bias voltage generating circuit is input to a source of the transistor of the linearization circuit, and the oscillation frequency control signal from the loop filter is input to a gate of the transistor, and

the conversion gain of the phase comparator and the charge pump circuit is continuously controlled, depending on a value of the current flowing through the transistor.

[7] The PLL frequency synthesizer of claim 6, wherein the transistor of the linearization circuit is composed of a plurality of transistors, and

the conversion gain of the phase comparator and the charge pump circuit is continuously controlled, depending on a sum of currents flowing through the plurality of transistors.

[8] The PLL frequency synthesizer of claim 7, wherein the bias voltage generating

circuit generates a plurality of different bias voltages, and

the different bias voltages from the bias voltage generating circuit are input to respective sources of the plurality of transistors of the linearization circuit.

[9] The PLL frequency synthesizer of claim 8, wherein the bias voltage generating circuit changes the plurality of generated bias voltages based on an externally input bias voltage setting signal.

[10] The PLL frequency synthesizer of any one of claims 4, 5, 7, and 8, wherein the plurality of transistors of the linearization circuit are composed of a P-type or N-type MOS transistor or P-type and N-type MOS transistors.

[11] The PLL frequency synthesizer of claim 2, wherein the linearization circuit comprises:

a voltage-current conversion circuit of converting a voltage of the oscillation frequency control signal from the loop filter into a current; and

a charge pump current control circuit of receiving the current from the voltage-current conversion circuit, generating a charge pump current control signal corresponding to a value of the received current, and outputting the charge pump current control signal to the charge pump circuit,

wherein the charge pump circuit regulates a flowing current based on the charge pump current control signal from the charge pump current control circuit.